12. A method for partial write for storing information in a device including an array of memory cells, said method comprising:

organizing the array with bitlines and wordlines for addressing the memory cells;

subdividing said bitlines into sectioned bitlines for sections of wordlines; and

connecting sectioned bitlines to one of global bitlines by a connector, said connector being bidirectional and using the high order part of the wordline addresses for a section of bitlines as a disable reset command such that the reset stays active for unselected portions of the array thereby compensating leakage of a mass of unselected memory cells which could disturb valid read signals.

13. The method according to claim 12, further comprising precharging said bitlines to power rail voltage.

14. The method according to claim 12, further comprising precharging said global bitlines to ground.

15. The method according to claim 12, further comprising delaying said disable reset command when writing to a memory cell thereby avoiding pre-setting the global bitline by reading the memory cell.

16. The method according to claim 12, further comprising splitting said disable reset command and controlling said reset command by the signals selecting one of several bitlines driving toward the memory output in order to maintain unselected bitlines in precharged condition.

17. The method according to one claim 12, wherein said bitlines and said global bitlines are both dual railed.